

Theoretical and Empirical Qualification of a Mechanical-Optical Interface for Parallel Optics Links

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ABSTRACT

As the implementation of parallel optics continues to evolve, development of a universal coupling interface between VCSEL/PD arrays and the corresponding photonic turn connector is necessary.

A newly developed monolithic mechanical-optical interface efficiently couples optical transmit/receive arrays to the accompanying fiber optic connector. This paper describes the optical model behind the coupling interface and validates the model using empirical measurements. Optical modeling will address how the interface is adaptable to the broad range of VCSEL/PD optical parameters from commercially available VCSEL hardware manufacturers; the optical model will illustrate coupling efficiencies versus launch specifications. Theoretical modeling will examine system sensitivity through Monte Carlo simulations and provide alignment tolerance requirements.

Empirical results will be presented to validate the optical model predictions and subsequent system performance. Functionality will be demonstrated through optical loss and coupling efficiency measurements. System metrics will include characterizations such as eye diagram results and link loss measurements.

Keywords: mechanical-optical interface, photonic turn connector, VCSEL, coupling efficiency, system link loss, optical theoretical model, board-level optics, transceiver

1. INTRODUCTION

As parallel optics continues to expand, driven by ever increasing data rates, there is a need to move towards mid-board level optics and connectors. While high-density connectors have improved card-edge spacing, mid-board level connections reduce and /or eliminate many of the problems that occur as transceiver modules become higher-speed and space constrained. Moving to miniature embedded fiber optic connectors allows the transceiver to be removed from the card edge, which leads to immediate gains in reduced electrical path lengths, simpler EMI and heat management, and significantly more board space for system architecture designs^{1,2}. While most transceivers launch perpendicular to the circuit boards, logistical space constraints necessitate the embedded fiber optic connectors maintain low profiles and efficiently rotate the light such that traditional fiber optic cable routing schemes can be implemented. Low profile photonic light-turn (PLT) connectors that rotate the light while coupling it efficiently into fiber optic cable largely solve many of the problems of moving the transceiver VCSELs and PDs to mid-board locations^{3,4,5}. However, in most cases, a coupling interface is still needed between the VCSEL and the PLT connector, as VCSEL sources are highly divergent and often difficult to access due to the wire-bonds and chip drivers located in close proximity. While the embedded connectors and fiber optic infrastructure are readily available, the availability of a standardized coupling interface has remained elusive, and most current solutions remain proprietary, expensive, or simply inefficient at coupling across a wide range of VCSEL design parameters. Any interface, while effectively coupling between a wide-range of VCSEL and PD designs, must also be able to mechanically secure the PLT connectors and be compatible with the transceiver space constraints.

A new mechanical-optical interface (MOI) has been developed to address the interface void between the VCSEL and PLT connectors. The MOI has been designed to satisfy both the mechanical and optical requirements for mid-level coupling between PLT connectors and the VCSEL/PD components commonly available.

2. MECHANICAL FEATURES

The MOI is a monolithic injection-molded component that is board-mounted above the VCSEL/PD to allow seamless mechanical coupling to the PLT connector. The MOI, shown in Figure 1, contains three features primarily associated with the optical performance of the component and several features for the mechanical alignment and constraint between the VCSEL/PD and PLT connector. On the bottom of the MOI is an array of lenses that are positioned directly over the VCSEL/PD components and four pedestals to control the height between the VCSEL/PD and the lens focal position. Opposite the lens array, on the top of the MOI, is an optically flat exit window where, on the Tx end, the collimated light leaves the MOI in route to the PLT connector.

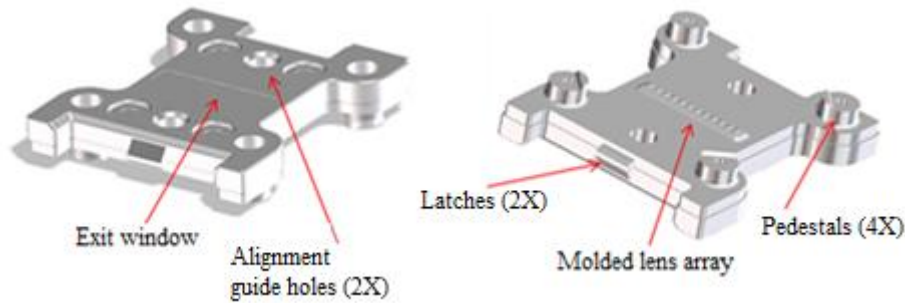


Figure 1. The MOI, with primary features indicated on both sides of the component.

For purposes of precise alignment, the MOI has been designed to be compatible with conventional die bonders. The pedestals, in addition to setting the MOI lens height, also control the epoxy bond-line thickness when the MOI is placed over the VCSEL/PD via the die bonder⁶. Once the MOI has been secured above the VCSEL/PD, the alignment guide holes and latches (shown in Figure 1) allow the PLT connector to be snapped into the MOI with micron-level alignment repeatedly and secured with the PLT housing, where the latches secure it in place^{7,8}. The general alignment of the MOI, PLT connector, and housing, as well as the optical path can be seen in Figure 2.

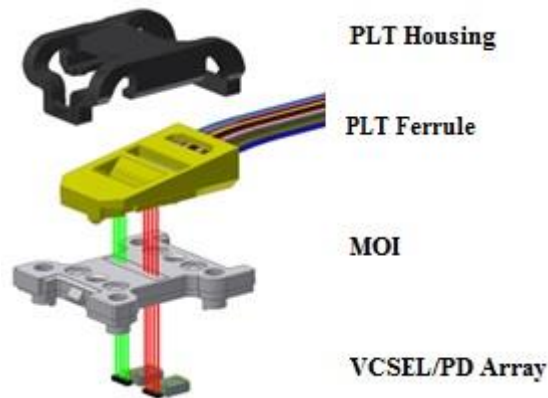


Figure 2. Alignment between the VCSEL/PD array, MOI, PLT connector, and PLT housing.

Once the MOI, PLT ferrule, and PLT housing have been combined, a clean optical path has been created from the VCSEL through to the optical fiber and can easily be coupled to the board edge, off the board, or to other necessary areas. The PLT connector is compatible with both traditional ribbon cable and loose tube round cable jumper assemblies, which are ideal for mid-board routing since round cable jumpers have no preferential bend issues^{4,9}. A cross-sectional schematic of a full VCSEL to PD link involving MOIs and PLT connectors is shown in Figure 3. The simulated optical path is indicated along with the Tx and Rx receive and launch points that were used for the optical modeling that will be discussed below.

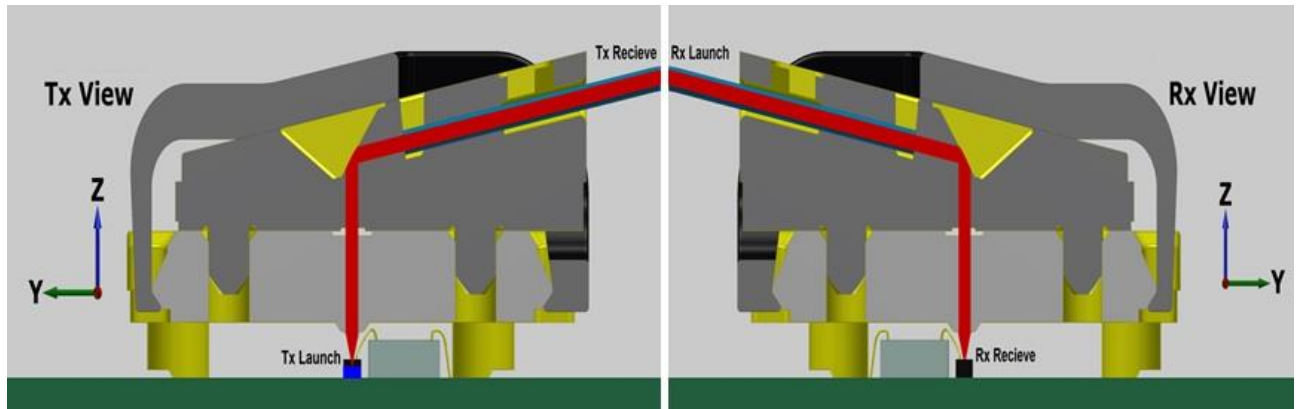


Figure 3. Cross-section view of a full Tx/Rx link involving VCSEL, MOI, PLT ferrule, housing, and fiber, and return trip to PD. The optical path is indicated.

3. OPTICAL MODELING

3.1 Design Assumptions

In order to design an interface that can optimally couple across a wide range of VCSEL and PD launch and receive conditions, Zemax was used for the optical modeling and optimization. During the design process, it was decided to design one lens prescription for both the Tx and Rx components; while this creates limitations on the optimization routines, it provides simplicity in a customer production environment in terms of die bonder programs, test procedures, inventory, and part identification. VCSEL coupling and alignment requirements proved to be much more sensitive than PD requirements due to the significantly smaller optical aperture diameters (Table 1), so the design concentrated on the VCSEL optimization. An industry survey of common VCSEL and PD dimensions and requirements quickly lead to the conclusion that space around the optical dies was at a premium in many applications; wire-bonds, copper traces, and chip drivers vary widely in terms of size, shape, and requirements. Therefore, one of the primary goals of the MOI design was to maximize the clearance between the MOI lenses and the surface of the VCSEL. The VCSEL launch divergence angle provides an upper limit on the lens location, since the lens array must be close enough to still capture the light and prevent crosstalk between adjacent channels. With the basic outline of the MOI constrained by VCSEL and PD requirements as shown in Figure 4, optimization was performed to maximize coupling efficiency while minimizing die bonding alignment requirements.

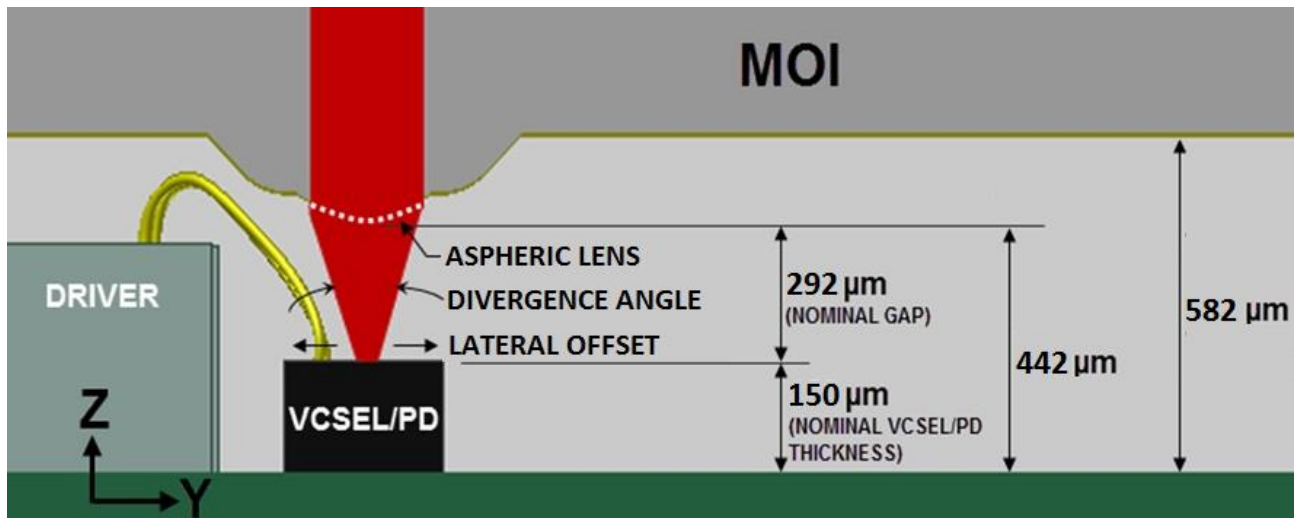


Figure 4. Cross-section of the MOI and VCSEL/PD, showing critical dimensions and variable definitions for the optical modeling process and results.

The same survey of commercially available VCSEL and PD arrays found that most optical parameters fell into a small operating range for both 10 Gb/s and 25 Gb/s components; the list of optical launch and receive parameters used for the subsequent optical design is shown in Table . All subsequent modeling and charts below assume 850 nm wavelength light, standard OM3 50/125 μm multi-mode fiber for the PLT connectors, and no anti-reflection (AR) coatings on any of the VCSEL, PD, MOI, or PLT surfaces. AR coatings can provide mitigation of back-reflection effects, multi-path interference, and improve link loss and will be addressed later in section 3.5. The two following sections discuss the Tx and Rx results individually, before combined link performance is examined in section 3.4. For both Tx and Rx performance, alignment sensitivity analysis is displayed for individual degrees of freedom using the launch and receive locations shown in Figure ; the combined effects are also shown as a Monte Carlo analysis in section 3.4.

Table 1. VCSEL and PD criteria used for MOI optical optimization.

	VCSEL Die Height	VCSEL Aperture Diameter	VCSEL Divergence Angle ($1/e^2$)	PD Die Height	PD Aperture Diameter
Nominal	150 μm	8 μm	25°	150 μm	35 μm
Max	200 μm	8 μm	32°	200 μm	55 μm
Min	130 μm	6 μm	20°	120 μm	30 μm

3.2 Tx Results

Tx performance is primarily a function of lateral offset between the MOI lens and the VCSEL. Figure 5a shows the change in insertion loss for different VCSEL divergence angles while the MOI lens is at the nominal 292 μm above the VCSEL surface. For a 25° divergence angle, a lateral misalignment of $\pm 6 \mu\text{m}$ causes no measurable change in loss performance; alignments of half that are reasonable with traditional die bonding equipment. Figure 5b shows that the Tx performance is insensitive to the gap between the VCSEL and MOI. Under normal conditions for a 150 μm tall VCSEL die, vertical alignment should only be impacted by bond line thicknesses during die placement of either the MOI or VCSEL; neither case should have any impact on insertion loss. Figure 5b can also be used to determine Tx performance for VCSELs of different heights; since $\pm 30 \mu\text{m}$ changes in height have almost no impact on performance, VCSELs ranging from 120-180 μm can be accommodated without any adverse impact to performance. Tilt between the MOI and VCSEL array or circuit board is shown in Figure c. Under normal die bonding procedures there is no impact due to tilt for any of the shown divergence angles. Most die bonders in the precision alignment industry hold substantially better than 2° angles.

3.3 Rx Results

On the Rx side of the system, the aperture diameter takes the place of the divergence angle as the primary driver of sensitivity. As with Tx, for typical mid-range diameter values for the PD aperture the lateral offset values should be easy to hold with a conventional die bonding system; from Figure 6a, for a 50 μm diameter PD only $\pm 10 \mu\text{m}$ lateral alignment must be maintained. Unlike the Tx side, height variation is more critical for Rx side; Figure 6b indicates that as the PD gets taller than 150 μm both lateral and vertical alignment become sensitive, but for PDs smaller than nominal, performance poses no problems at all. As with the Tx side, the MOI/PD alignment is highly insensitive to tilt, as can be seen in Figure 6c.

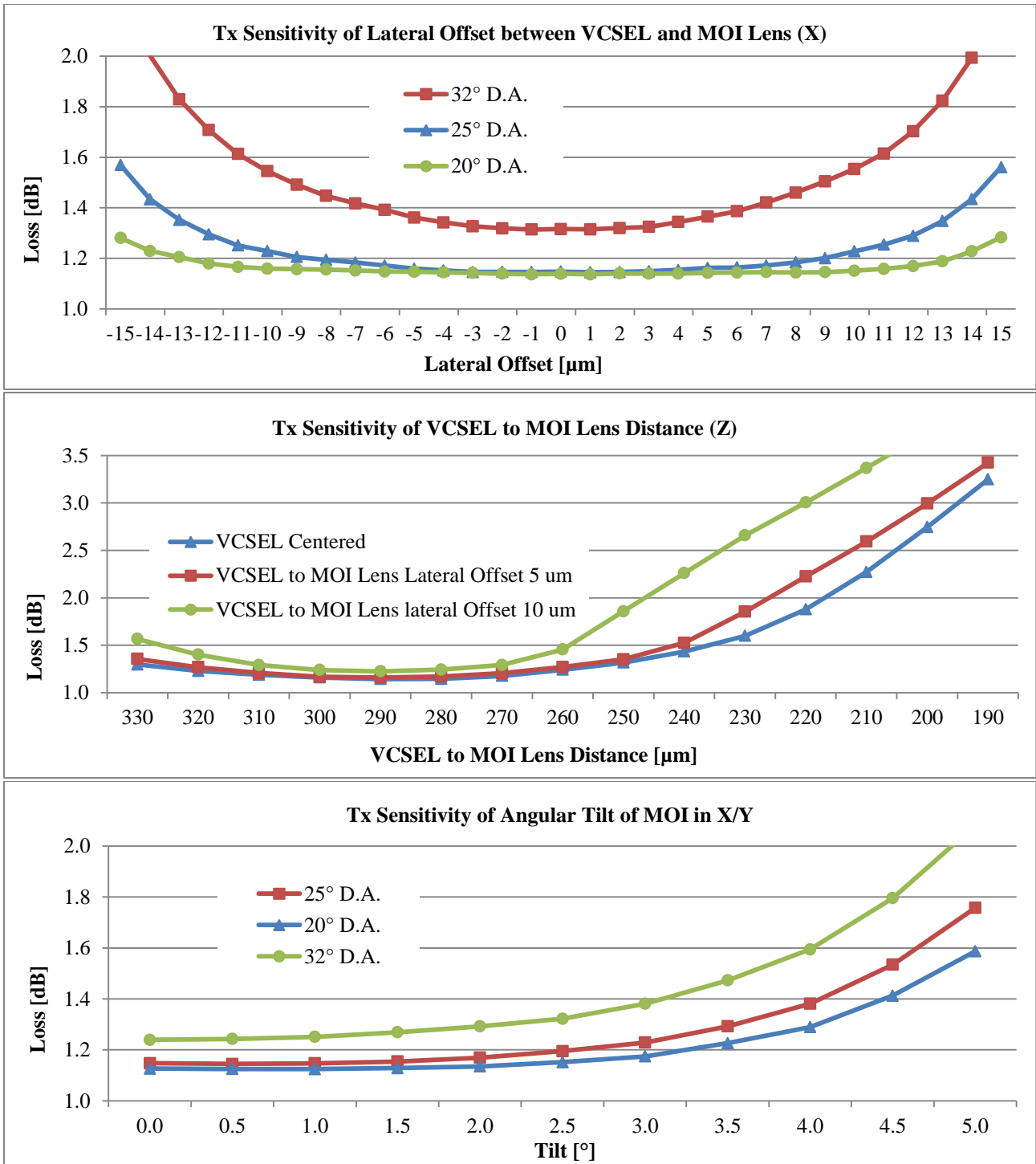


Figure 5. Tx sensitivity of misalignment between a MOI lens and the VCSEL; a) lateral misalignment as a function of divergence angle of the VCSEL, b) vertical misalignment in conjunction with lateral misalignment, and c) tilt between the MOI and VCSEL array as a function of divergence angle of the VCSEL.

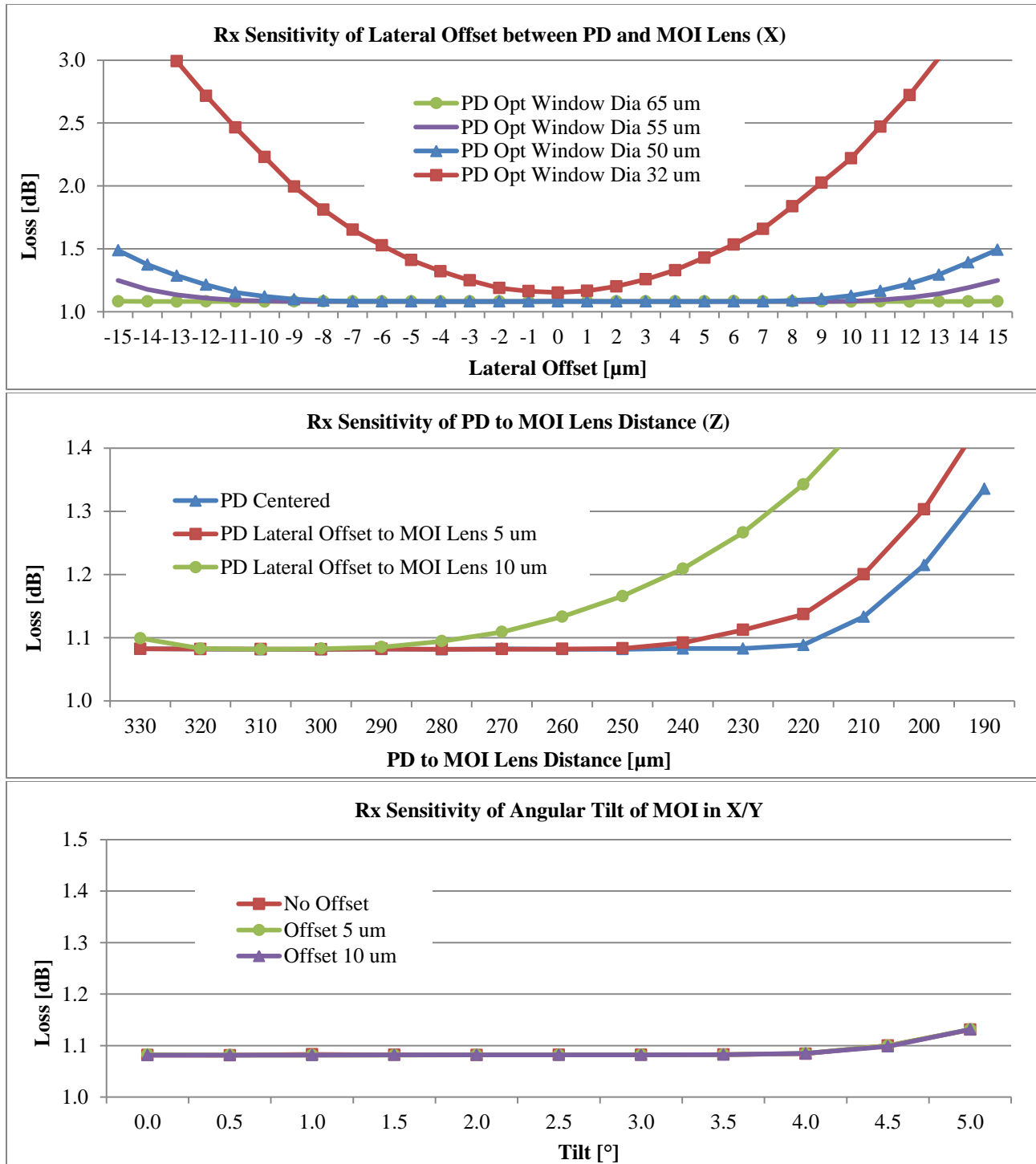


Figure 6. Rx sensitivity of misalignment between a MOI lens and the PD; a) lateral misalignment as a function of PD aperture diameter, b) vertical misalignment in conjunction with lateral misalignment, and c) tilt between the MOI and PD array in conjunction with lateral misalignment. A 10 μm misalignment between MOI and PD has no discernable impact on tilt, as such all three data sets overlap each other completely.

3.4 System Results

While it is important to understand the individual sensitivity of each degree of freedom of the previous sections for die bonding purposes, link loss performance is more adequately determined via Monte Carlo analysis. For both Tx and Rx configurations, Monte Carlo calculations were run assuming normal distributions for the ranges in Table 2, using 500 trials each.

Table 2. Variables and values used for Monte Carlo simulations for MOI performance.

Tolerance Item	Nominal	Min	Max
VCSEL to MOI Lens - Lateral Offset	0 μm	-10 μm	+10 μm
VCSEL to MOI Lens - Distance	292 mm	272 μm	312 μm
VCSEL to MOI Lens - Tilt	0 $^\circ$	- 1 $^\circ$	+ 1 $^\circ$
VCSEL Beam - Divergence Angle	25 $^\circ$	20 $^\circ$	32 $^\circ$
VCSEL Aperture Size	8 μm		
PD to MOI Lens - Lateral Offset	0 μm	-10 μm	+10 μm
PD to MOI Lens - Distance	292 mm	272 μm	312 μm
PD to MOI Lens - Tilt	0 $^\circ$	- 1 $^\circ$	+ 1 $^\circ$
PD Aperture Size	55 μm		

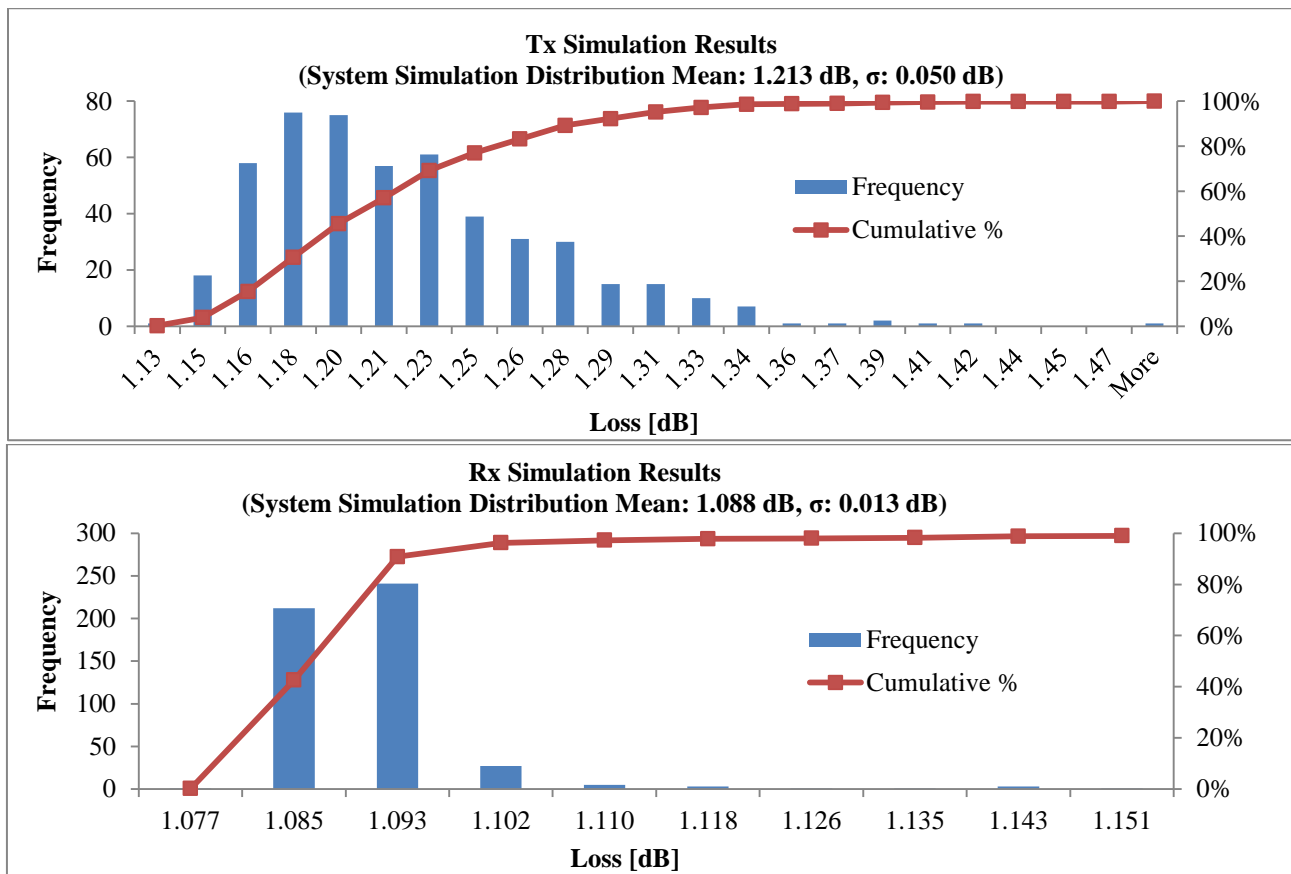


Figure 7. Monte Carlo simulations of a) Tx and b) Rx link loss performance assuming normal distribution and 500 trials each.

The Tx Monte Carlo results, shown in Figure 7a, indicate that the mean loss is approximately 1.21 dB, with 99.7% of the results under 1.37 dB. The Rx link in Figure 7b, being less sensitive to alignment, has an average loss of 1.09 B with three sigma performance of 1.13 dB.

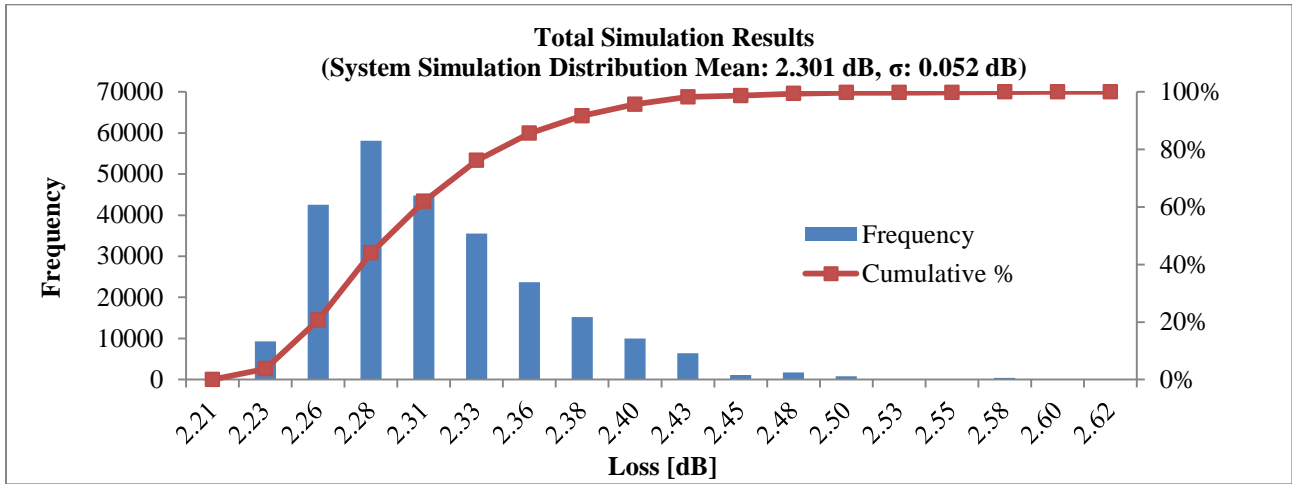


Figure 8. Monte Carlo prediction of the full system link, using the Tx and Rx from Figure convolved together.

To determine a full link performance, the 500 trials from the Tx Monte Carlo run were convolved with the 500 Rx trials, resulting 250,000 trials in the link budget shown in Figure 8Figure ; a full link has an average loss of 2.3 dB with a three sigma upper limit of 2.46 dB.

3.5 AR Coating Results

While the total link loss above is quite acceptable for most applications, there are a number of surfaces in the optical path where power is lost due to the air/plastic interfaces, most notably the flat optical exit window of the MOI and the PLT connector. AR coatings can be applied to both surfaces to reduce the reflected light and eliminate any concerns of multi-path interference (MPI). To date, there has not been any indications that MPI exists as an issue for PLT connectors; there are many cases of PLT connectors with exposed optical exit windows achieving very good performance results at high data rates, although the optical window opposite the PLT connector was likely AR coated in some of those cases^{10 11 12}. However, should the need exist to improve performance; Table 3 indicates the level of improvement at each surface that is AR coated, assuming 850 nm coatings, and Table 4 displays the adjusted average insertion loss expected from the Monte Carlo results previously.

Table 3. Theoretical insertion loss improvement per AR coated surface in the full link.

AR Coated Surface	Tx Reduction in Loss (dB)	Rx Reduction in Loss (dB)
MOI lens	0.20	0.20
MOI optical window	0.23	0.22
PLT optical window	0.20	0.20

Table 4. Expected average insertion loss performance from Monte Carlo results without AR coatings, and with AR coating on the MOI exit window surface.

Component	Tx Average (dB)	Rx Average (dB)	Total link Average (dB)
No AR coating	1.21	1.09	2.30
AR coated MOI window	0.99	0.87	1.85

4. EXPERIMENTAL RESULTS

4.1 Insertion Loss Testing

To validate the theoretical model with empirical results, 10 independent MOIs were aligned and attached to QSFP PCB assemblies using standard commercially available die bonding equipment. The PCB assemblies were already fully populated with 14Gbps VCSEL arrays (1x4), PD arrays (1x4), amplifiers (TIA) and drivers. The die bonder had a listed XY axis accuracy of $\pm 3 \mu\text{m}$ at 3 sigma. All of the MOI components were AR coated on the exit window only.

Prior to MOI attachment, each VCSEL was powered and a large area detector was used to verify baseline power output, P_1 , which averaged 3.0 dBm. A MOI was then affixed to the PCB assembly and a PLT connector and associated optical test circuit shown in Figure 9 were attached. Power readings were then taken at the P_2 point at the LC connection with a wide area detector, and again with the PD array at point P_3 . These measurements were repeated for all four channels of each of the ten PCB boards. The insertion loss results distributions are shown in Figure along with normal probability plots. Monte Carlo trials had assumed normal distributions for all variables; the probability plots tend to validate this assumption, although the small sample size ($n=40$) clearly is a limiting factor.

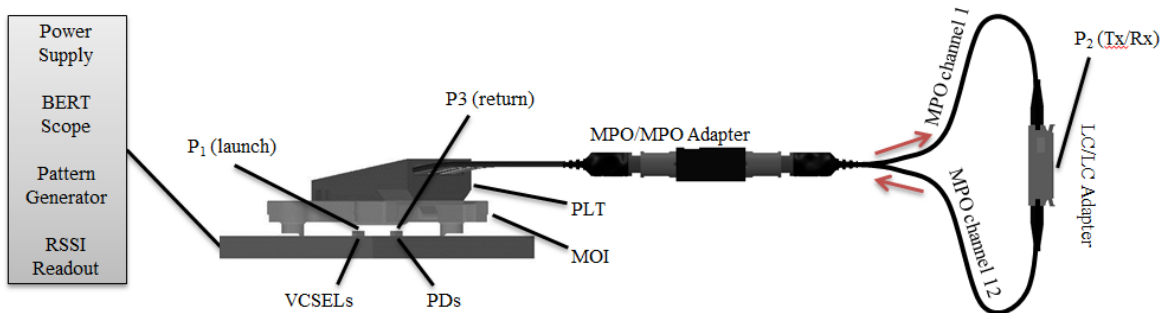


Figure 9. Schematic for empirical testing of insertion loss of MOI and associated link. P_1 indicates the reference power exiting the VCSEL, P_2 is the power measured via wide-area detector, and P_3 is the power measured on return by the PD.

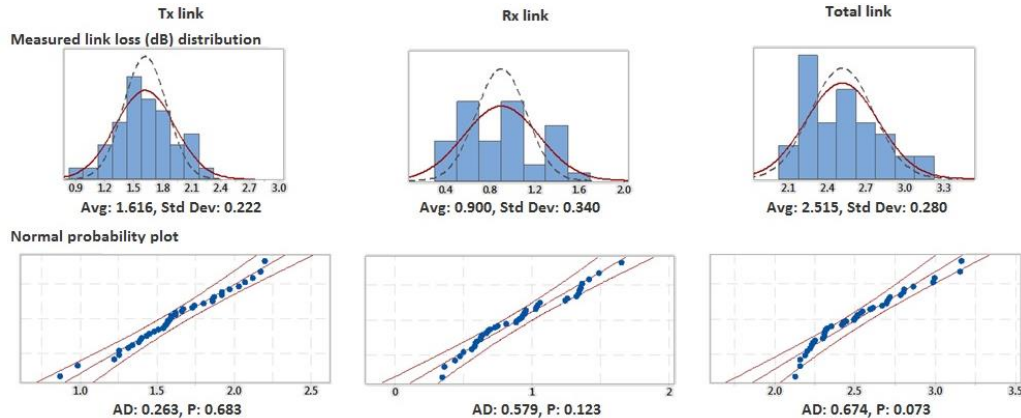


Figure 10. Measured insertion loss performance for all ten MOI/QSFP links. All loss values in dB.

The optical Zemax model assumed a detector placed within the optical fiber; therefore, the extra MPO, LC and reflection losses of the experimental measurements need to be accounted for before a comparison can be made. When comparing the power readings to the optical model, the Tx system is simply $P_1 - P_2$; however there is an extra loss at the MPO/MPO connection and a reflection at the LC connector interface when it is placed in front of the detector. Similarly, the Rx system is $P_2 - P_3$, but has several interfaces that must be compensated for; the reflection from the exposed LC connector is removed, but there is still an LC/LC connection and a MPO/MPO connection. Finally, the total system link is $P_1 - P_3$. Table 5 shows the theoretical model average values from the Monte Carlo results, the expected insertion loss improvements in performance due to the AR coating, and typical losses expected from connectors and fiber reflections¹³
¹⁴ ¹⁵

Using the expected values for each connector and reflection surface, the expected average results from the theoretical model would be 1.32 dB, 1.10 dB, and 2.45 dB for the Tx, Rx, and full system links respectively. In each case, the average measured value differed from the expected value by 3% or less, showing very good correlation between the empirical results and the predicted values.

Table 5. Theoretically expected average loss values, adjusted for fiber optic connections in test setup. The final two rows displays the average measured data and percent difference (in mW) from the theoretically adjusted values.

	Tx	Rx	Total link
Theoretical model value (dB)	1.21	1.09	2.30
Expected AR change (dB)	-0.23	-0.22	-0.45
Expected MPO loss (dB)	0.20	0.20	0.40
Expected LC loss/reflection (dB)	0.17	0.03	0.20
Adjusted model expected value (dB)	1.35	1.10	2.45
Average measured value (dB)	1.62	0.90	2.52
Average percent difference (in mW)	3.0%	-2.3%	0.8%

4.2 Eye Diagram Results

While the insertion loss results validate the theoretical model, neither the model or insertion loss data truly address system performance. Therefore, the pattern generator integrated into the PCB assembly board was used to test the full system link at both 10 Gbps and 14 Gbps per channel using the setup shown in Figure 9. Oscilloscope screenshots in Figure 11 show that the link was in full compliance with the QSFP mask specification at both speeds.

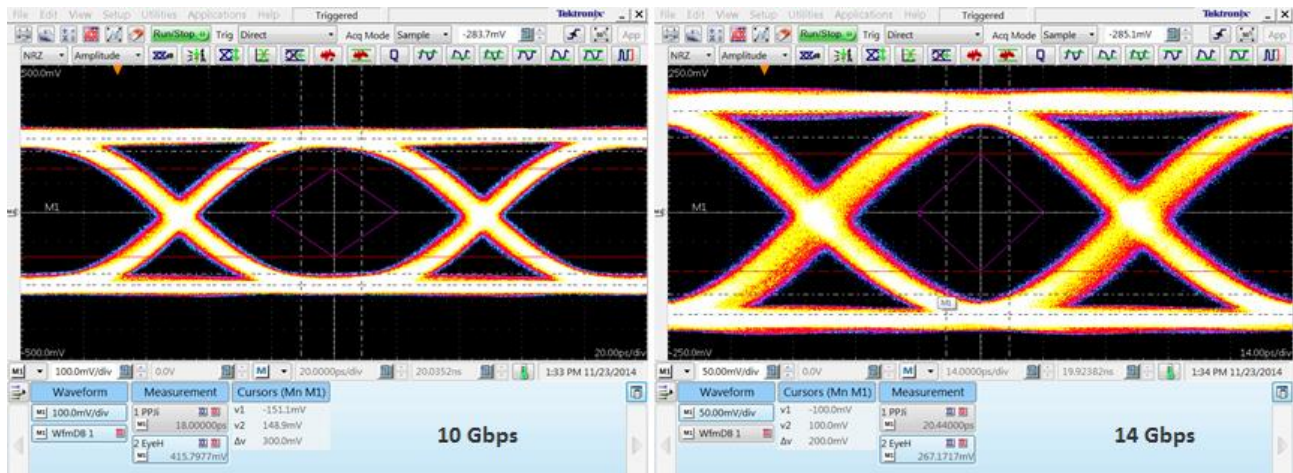


Figure 11. Full link system results at 10 Gbps and 14 Gbps per channel show full compliance with QSFP mask specification.

5. SUMMARY

To support the expanding need for mid-level optical interconnects, a mechanical-optical interface has been developed that acts as a coupling component between the VCSEL/PD active optics and the PLT connectors that lead into the remainder of the passive optical network. A theoretical model has been developed and optimized over the current range of VCSEL and PD optical characteristics that exist in the marketplace today. Sensitivity analysis using the theoretical model shows that component alignment and placement using standard die bonders is readily achievable. To validate the Zemax modeling, ten components were die bonded to QSFP PCB assemblies and run through insertion loss and eye-

diagram testing. The average measured insertion loss performance for the Tx, Rx, and full system were all well within 5% of the theoretically predicted values. Eye diagrams showed that the full link was compliant with the QSFP mask specifications while running at 14 Gbps per lane.

Future development of the MOI component may include support for higher data rate applications through either integrated reflection mitigation features on the lenses and exit windows and/or support for higher channel counts; currently the IEEE 802.3bs working group is developing 16 channel schemes for 400 Gbps applications¹⁶. As data rates continue to climb, it is expected that PD apertures will shrink and VCSEL beam outputs will further diverge, which may necessitate a new lens prescription to support smaller spot diameter requirements. Similarly, with a different lens prescription, nothing precludes the MOI from supporting coupling for single-mode fiber applications, although the alignment sensitivity analysis would have to be studied carefully.

REFERENCES

- [1] Fields, M., "Transceivers and Optical Engines for Computer and Datacenter Interconnects," OFC/NFOEC 2010 Special Symposia, "Beyond Telecom and Datacom: Optical Interconnects for the Computer Era," (2010).
- [2] Vaughan, D., Hannah, R. and Fields, M., "Applications for Embedded Optic Modules in Data Communications," 25 March 2011, <<http://www.avagotech.com/docs/AV02-2869EN>> (6 January 2015).
- [3] Childers, E., Graham, J., Hughes, M., Schoellner, D. and Ugolini, A., "Miniature detachable photonic turn connector for optical module interface," IEEE 61st Electronic Components and Technology Conference, (2011).
- [4] Childers, D., Childers, E., Graham, J. and Hughes, M., "Next-generation, high-density, low-cost, multimode optical backplane interconnect," Proc. SPIE 8267 Optoelectronic Interconnects XII, (2012).
- [5] Peng Li, M., Martinez, J. and Vaughn, D., "Transferring High-Speed Data over Long Distances with Combined FPGA and Multichannel Optical Modules" 21 March 2012, <<http://www.avagotech.com/docs/AV02-3383EN>> (6 January 2015).
- [6] Chuang, S., Schoellner, D., Ugolini, A., Wakjira, J. and Wolf, G., "Development and qualification of a mechanical-optical interface for parallel optics links," Proc. SPIE Photonics West: Optical Interconnects XV, (2015).
- [7] Hughes, M., Graham, J., Schoellner, D., Childers, D., Childers, E. and Ugolini, A., "Miniature Detachable Photonic Turn Connector for Parallel Optic Transceiver Interface," OFC/NFOEC 2011, (2011).
- [8] Childers, E., Hastings, D., Schoellner, D., Ugolini, A. and Wakjira, J., "Performance methodologies of a modular miniature photonic turn connector," Proc. SPIE 8630 Photonics West: Optoelectronic Interconnects XIII, (2013).
- [9] Smith, T., and Bishop, G., "Ribbon vs. Loose Tube Fiber Cabling," NFOEC 2006, (2006).
- [10] Benner, A., Kuchta, D., Pepeljugoski, P., Budd, R., Hougham, G., Fasano, B., Marston, K., Bagheri, H., Seminaro, E., Xu, H., Meadowcroft, D., Fields, M., McColloch, L., Robinson, M., Miller, F., Kaneshiro, R., Granger, R., Childers, D., and Childers, E. "Optics for High-Performance Servers and Supercomputers," OFC 2013, "Beyond Telecom and Datacom Symposium III," (2010).
- [11] Iles, G., Jones, J., and Rosea, A., "Experience powering Xilinx Virtex-7 FPGAs," Topical Workshop on Electronics for Particle Physics, (2013).
- [12] Kuchta, D., Rylyakov, A., Schow, C., Proesel, J., Baks, C., Westbergh, P., Gustavsson, J., and Larsson, A., "64Gb/s Transmission over 57m MMF using an NRZ Modulated 850nm VCSEL," OFC 2014, "Low Power VCSEL Interconnect," (2014).
- [13] US Conec, Ltd, "MT Ferrule Kits," 2011, <<http://www.usconec.com/products/ferrules/mt-ferrule-kits.htm>> (7 January 2015).
- [14] Corning, Inc., "Corning ClearCurve Multimode Optical Fiber," 2011, <<http://www.corning.com/WorkArea/downloadasset.aspx?id=36549>> (7 January 2015).
- [15] Molex, "Fiber Optic Products," 2015, <http://www.molex.com/catalog/web_catalog/pdfs/Q.pdf> (7 January 2015).
- [16] Kolesar, P., Lingle, R., and Ugolini, A., "400GBASE-SR16 Cabling," September 2014, <<http://www.ieee802.org/3/400GSG/email/pdf2XrN5gMdmE.pdf>> (7 January 2015).