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Detachable 1x8 Single Mode Optical Interface for DWDM Microring Silicon Photonic Transceivers

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ABSTRACT

We are developing a 1x8 single mode (SM) optical interface to facilitate the adoption of dense wavelength division multiplexing (DWDM) silicon photonic (SiPh) optical interconnects in exascale computing systems. A common method for fiber attachment to SiPh transceivers is 'pigtailing'- the permanent adhesive bonding of fiber/v-groove arrays to on-chip grating couplers (GC). This approach precludes standard high throughput surface mounting and solder reflow assembly of the transceiver onto system printed circuit boards. Our approach replaces the fixed pigtail with a low profile, small form factor, detachable expanded beam optical connector which consists of four essential parts: a GC array, a surface mount glass microlens array chip, an injection molded solder reflowable optical socket, and an injection molded SM light turn ferrule. The optical socket and ferrule are supplied by US Conec Ltd. To design the GC, we developed an optical simulator that considers CMOS foundry constraints in the optimization process. On-wafer measurements of the GC coupling loss to SMF28 fiber at 1310nm is ~1.4dB with a 1dB bandwidth of ~22nm. This ensures a wide low loss spectral window for at least 16 DWDM channels. The geometry of the optical system is arranged so that only a simple spherical lens is required for efficient mode matching in the expanded beam space. The fiber to fiber insertion loss through the light turn ferrule, two microlenses and GCs, and a looped back SOI waveguide ranged from 4.1-6.3dB, with insertion loss repeatability of 0.2dB after multiple mating cycles.

Keywords: silicon photonics; optical interconnects; optical connector; single mode fiber; grating coupler; optical packaging; DWDM; microring

1. INTRODUCTION

A practical exascale high performance computer must process, transport and store a tremendous amount of data without exceeding a power envelope of 20-50MW. High bandwidth energy efficient communication is paramount to achieve this goal. Silicon photonics (SiPh) is one potential technology that can satiate the bandwidth of an exascale system without breaking its power budget [1] [2]. Although fiber optic links are replacing copper for medium distance communication, they are not ubiquitous in high performance computer (HPC) network fabrics. To reap the benefits of fiber optic links, it is necessary to reduce the distance between the photonic components and the network switch. The reduction in distance improves signal integrity and power consumption. This process is already under way with the move from active optical cables (AOC) to mid-board optics [3] to co-packaged optics [4]. Our goal is to develop modular technologies to co-package SiPh interposers with application specific integrated circuits (ASIC) and other high input/output (IO) bandwidth density components for exascale systems and HPC.

A wide variety of SiPh building blocks, e.g., grating couplers (GC), microring resonators, arrayed waveguide gratings, optical modulators, photodetectors, etc., have been established at research and development (R&D) and commercial CMOS foundries, and are available through multi-project wafer (MPW) or dedicated fabrication runs [5][6][7][8]. One key challenge is achieving low cost, resilient, efficient light coupling between single mode fibers (SMF) and submicron silicon on insulator (SOI) waveguides. As shown in Figure 1, due to their size difference, the mode field area in the SMF must be reduced by a factor of ~700 to match the fundamental mode in the SOI waveguide. Three approaches have been proposed to confront this issue: edge waveguide taper, grating, and evanescent coupling [9]. Among these, GCs are attractive due to their reasonable footprint (~10x10μm^2), wide optical bandwidth (>20nm), on-chip placement flexibility, and compatibility with wafer scale optical testing.

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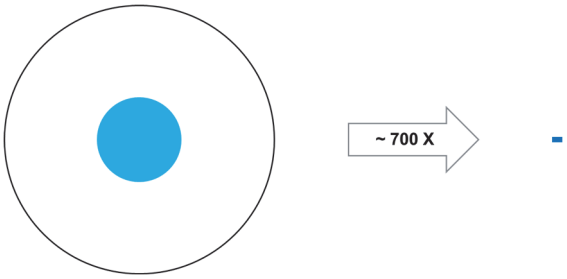


Figure 1: Area mismatch between a single mode fiber (left) and submicron silicon on insulator waveguide (right).

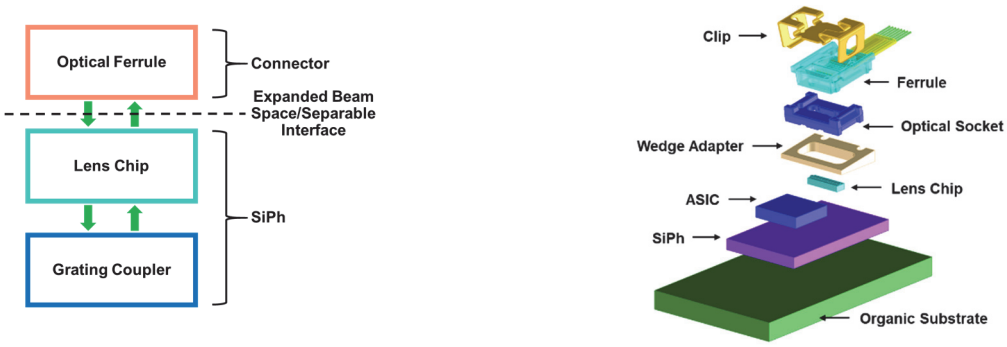
Optical interfaces with linear GC arrays mode matched to SMFs, mounted in v-groove arrays, have received wide acceptance as an industrial solution [10]. To ensure efficient coupling, the lateral alignment precision between the GC and SMF arrays must be less than ±1µm. The primary solution from industry to achieve this level of precision is active alignment, which requires laser operation and optical power monitoring, combined with permanent attachment of the SMF/v-groove array. This precludes the possibility for surface mount assembly of electronic components co-packaged or tightly integrated with SiPh transceivers by standard solder reflow processes due to the presence of the dangling fiber pigtail.

Our approach replaces the fixed pigtail with a low profile, small form factor detachable expanded beam optical connector. The ability to remove and re-attach the optical connector ensures flexibility in component placement on system printed circuit boards (PCB), easy replacement of damaged fibers in the field, and enables the optimization of fiber length, for specific use cases, without the need for additional optical jumper cables and connectors. Our optical interface consists of four essential parts: a single polarization GC array, a surface mount solder reflow compatible glass microlens array chip and injection molded optical socket, and an injection molded 1x8 expanded beam single mode (SM) light turn ferrule. The optical socket and ferrule are supplied by US Conec Ltd [11].

2. OPTOMECHANICAL ASSEMBLY

2.1 Overview

The detachable single mode optical interface couples light between a 1x8 SMF28 fiber ribbon and a SiPh interposer. The block diagram of the optical interface, optical connector attached to the SiPh and its exploded view are shown in Figure 2. We have minimized the number of elements to implement the interface to the following: a glass lens chip, wedge adapter, optical socket, expanded beam SM light turn ferrule and clip. The optical interface is separable in the expanded beam space where the x-y-z alignment is relaxed at the expense of angular alignment. The expanded beam minimizes the losses associated with dust in the optical path at the separable interface and the connector engagement force compared to physical contact optical connectors [11]. These qualities are quite important for co-packaged optics to be deployed in real systems.



(a) (b)

Figure 2: Detachable single mode optical interface (a) block diagram and (b) optomechanical assembly exploded view.

The ferrule incorporates a total internal reflection (TIR) turning lens that redirects the light by 90deg and collimates the SMF mode to ~50µm diameter in the expanded beam space [11]. The wedge is intended to seat the optical socket at 8deg, which corresponds to the light beam exit angle from the lens chip relative to the plane of the SiPh interposer. The metal

clip seats and latches the ferrule into the socket, and protects the TIR lens on the ferrule. The lens chip, optical socket and adhesives are designed or selected to be compatible with standard lead free solder reflow processes. The glass lens chip is CTE matched to silicon and affixed to the SiPh with low shrinkage index matching underfill, while the optical socket is injection molded with a high temperature resin capable of withstanding exposure to multiple solder reflow cycles.

2.2 Optical Model

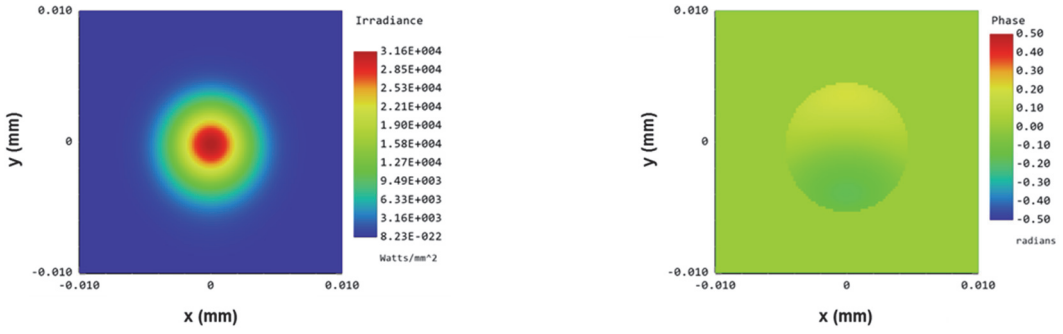
From an optical point of view, the basic function of the optical interface is to perform 1:1 imaging of the SMF mode onto the GC on the SiPh. The schematic of the optical system is shown in Figure 3. The green arrow in the schematic represents the chief ray that propagates along the optical axis of the system. The ferrule is tilted 8deg with respect to the SiPh plane and incorporates a turning lens that reflects the chief ray by 90deg. The turning lens also magnifies and collimates the SMF mode to enable large lateral (x, y) and longitudinal (z) misalignment tolerance between the ferrule and the lens chip. The lens chip focuses the expanded beam onto the GC and is positioned so the chief ray travels along the GC optical axis which is also tilted 8deg. This optical geometry enables the use of a simple spherical lens which is much easier to manufacture and inspect than an aspheric lens.

(a) (b)

Figure 3: Optical system (a) schematic and (b) OpticsStudio model.

The optical system was modelled in OpticsStudio using the physical optics propagation method. The input light beam from the SMF was approximated as a Gaussian with beam waist equal to 4.6µm at 1310nm wavelength. All materials and interfaces were considered ideal with no absorption and scattering loss, respectively. The output surface or receiver was located at the GC entrance and tilted by 8deg. The receiver mode was also approximated as a Gaussian with beam waist equal to 4.6µm on the tilted output surface. The lens chip prescription, GC and ferrule locations relative to the lens chip were optimized to maximize the coupling efficiency from the SMF to the GC. To ensure the lens chip is manufacturable, the glass substrate thickness was appropriately specified.

The irradiance and phase profiles of the beam at the GC are plotted in Figure 4. The beam at the GC entrance is slightly asymmetric, but has a relatively flat phase front. The beam waists along the x and y-directions are 4.4 and 4.8 µm, and the geometric coupling efficiency is 99%, corresponding to insertion loss of 0.04dB.



(a) (b)

Figure 4: Light beam (a) irradiance and (b) phase profiles at the grating coupler entrance.

2.3 Sensitivity Analysis

After optimizing the design in OpticsStudio, sensitivity analysis of a single optical channel was performed to identify the tolerance values for each design parameter that results in 0.25dB insertion loss. In general, there is a tolerance trade-off between translational (x, y, z) and angular (Θ_x, Θ_y) misalignment. Since the ferrule is an US Conec proprietary part, its manufacturing tolerances were not included. First, we looked at the sensitivity of the optical system to changes in the glass microlens radius of curvature (ROC). A relative ROC error of ±4% leads to a coupling loss of approximately 0.25dB. This amount of error in ROC is within the capability of our lens manufacturer. Next, with the lens chip fixed at its nominal location, we examined the alignment sensitivity of the ferrule and GC. The ferrule mating plane was tilted by 8deg relative to the SiPh, and its pivot point was located where the chief ray intersects the ferrule's exit surface. In the expanded beam region between the ferrule and lens chip, the translational sensitivity is relaxed at the expense of angular sensitivity. The z-tolerance (along the optical axis) is greater than ±600µm, the x and y tolerances (along the mating plane) are ±7µm, but the tilt angle Θ_x and Θ_y (tilt about the x and y-axes, respectively) tolerances are approximately ±0.25deg. At the image plane located at the GC, the expanded beam was focused to a spot size ≈ 9.2µm. The GC x-y plane was parallel to the SiPh interposer, and its pivot point was located where the chief ray exiting the GC intersects its output surface. Since the beam is small, the angular sensitivity is relaxed at the expense of translational sensitivity. The GC to lens z-tolerance (perpendicular to the SiPh interposer) is about ±6µm, the x and y tolerances (parallel to the SiPh interposer) are about ±1µm, but the tilt angle Θ_x and Θ_y tolerances are approximately ±1.1deg. These results highlight the positioning and manufacturing precision required of the glass microlens array chip, optical socket and ferrule to enable low insertion loss from fiber to SiPh.

2.4 Assembly Approach

The objective of the optomechanical assembly process is to establish a detachable optical interface between a SM multi-fiber lensed plastic ferrule and an array of GCs fabricated on the SiPh interposer. Two additional components play a key role in low insertion loss between the GCs and fibers; 1) a glass microlens array, which is vision-aligned and fixed to the SiPh and 2) an optical socket, also mounted above the SiPh surface, which mechanically accepts and positions the ferrule with respect to the paired arrays of lenses and GCs.

The assembly process leveraged existing surface mount methods. The glass lens chip was manually aligned to the SiPh with a FineTech Fineplacer Lambda. The first step in aligning the microlens array to the GC array was to set up the flip chip assembly tool to place lens chip at the target height with respect to the SiPh surface. Next, four drops of thixotropic light cure adhesive was dispensed onto the SiPh substrate in positions corresponding to the approximate final position of the lens chip corners. The SiPh interposer and lens chip were then placed onto the working surface of the flip chip aligner. The lens chip was picked up with a vacuum tool and rotated 90deg into a vertical position, allowing the aligner's split optic to simultaneously view the microlens and GC arrays. Fiducials on the SiPh interposer were then aligned with respect to fiducials on the static lens chip. The vacuum tool was then rotated 90deg into its final position, placing the lens chip onto the prepositioned glue drops. An adhesive curing lamp was switched on and the lens chip was temporarily affixed to the SiPh. The final step in the lens chip attachment process was to underfill and cure a transparent adhesive, with refractive index matched to the lens substrate material, between the lens chip substrate and SiPh surface. Since the ferrule and optical socket from US Conec were designed for 90deg light turn and direct mounting onto the SiPh surface, respectively, a machined wedge adapter was utilized to orient the light turn angle and optical socket to match the emission angle of the GC on the SiPh. The wedge adapter was glued to the SiPh surface after the lens chip was surface mounted. For higher volume production, the wedge adapter may be eliminated by designing and injection molding the solder reflowable optical socket to the required geometry.

The second step in the optical interface assembly was to semi-actively align and affix the position of the optical socket on the wedge adapter mounted on the SiPh. The meaning of the term 'semi-active' will be made clear shortly. This assembly process was done on an automated machine designed and built in-house. The subassembly from the first step, consisting of the SiPh interposer, with an aligned lens chip surrounded by the wedge adapter, was loaded onto a 6-axis hexapod. A multi-fiber cable, terminated in a SM light turn ferrule, was inserted and clipped into the optical socket. This subassembly was loaded into a holding clamp attached to a linear stage that moves the ferrule above the SiPh subassembly. An unpolarized 1300nm super luminescent light emitting diode (SLED) and large area detector (LAD) were connected to the outer fiber channels 8 and 1, respectively. The SiPh was provisioned with a looped back waveguide for 'semi-active' alignment. Light coupled to fiber channel 8 was directed through the ferrule, lens chip, GC and on-chip looped back waveguide, and back to fiber channel 1 (Figure 5).

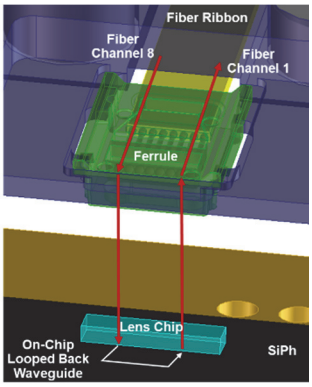


Figure 5: Lightpath between fiber ribbon and SiPh.

The hexapod performed a coarse x-y scan, in order to get first light, followed by a gradient decent algorithm to maximize the transmission between the outermost fiber channels. Then, the SLED was replaced with a 1300nm tunable laser and a polarization controller was engaged to optimize the insertion loss. This alignment process is deemed 'semi-active' because, while it does optimize alignment by maximizing received optical power, there is no need to provide electrical power to active optical devices on the SiPh. This greatly reduces the process complexity, often required in typical active alignment processes. Additionally, performing the alignment in the expanded beam space can compensate, to a certain extent, the lateral (x, y) and angular (Θ_x, Θ_y) misalignment between the microlens and GC arrays.

After the alignment process was repeated with the laser and finalized, the ferrule-optical socket subassembly was retracted, and a glue dispenser was extended to place drops of light cure adhesive onto the perimeter of the wedge adapter. Then, the subassembly was returned to the aligned position, the insertion loss was verified and, if necessary, alignment was repeated. Light guided adhesive curing sources were energized and the optical socket was temporarily affixed to the wedge adapter surface. The final step in the process involved dispensing and curing underfill adhesive between the underside of the socket and the wedge adapter surface. At this point, the optical jumper can be detached from the optical socket, and reattached multiple times with good repeatability in measured insertion loss.

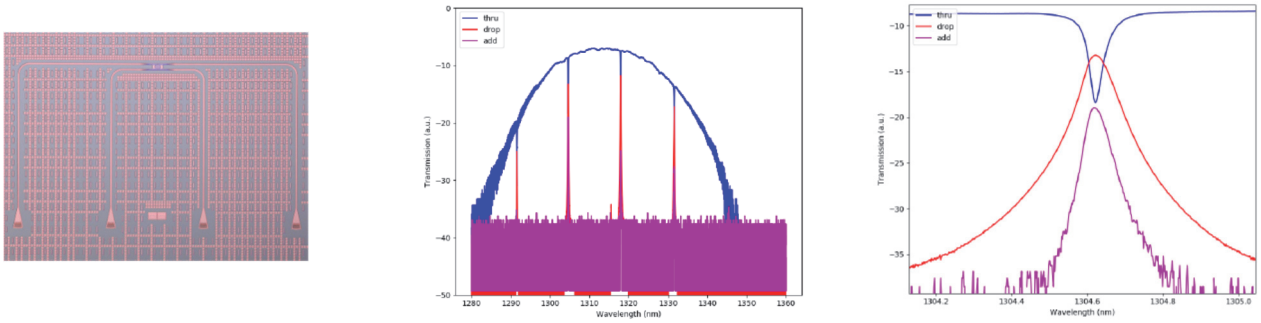
3. PHOTONIC COMPONENTS

3.1 SiPh Components

GCs and microring resonators are crucial building blocks for the dense wavelength division multiplexing (DWDM) SiPh transceiver. Every time light enters or leaves the transceiver, it passes through a GC. Consequently, reducing their coupling loss is critical in improving the optical link power budget. Silicon microring resonators are compact, versatile photonic devices [12]. They have a simple geometry, can be quite small (radius ~5μm) and densely packed due to the high refractive index contrast of SOI waveguides, and perform multiple functions such as optical multiplexing/demultiplexing and high speed modulation.

To design the GC, we used a finite difference frequency domain (FDFD) simulator based on adjoint optimization assuming 1310nm center wavelength and coupling to an 8deg angled SMF28 fiber [13][14]. The optimization algorithm considers geometric constraints due to real world CMOS foundry and SOI substrate manufacturing limits and tolerances. As the relevant physics of single polarization GCs are essentially 1D, we ran the adjoint optimization tool using fast 2D simulations instead of more time consuming full FDTD 3D simulations. Given a particular SOI substrate cross section and no constraints on the GC bar and groove dimensions, we obtained a coupling efficiency of 89% (-0.52dB), while the reflection was -41dB at the center wavelength. Using this structure as the initial condition and enforcing 65nm linewidth constraint, we re-optimized the GC geometry. The coupling efficiency dropped to 87% (-0.60dB), while the reflection at the peak wavelength improved to -43dB. Additional analysis confirmed that the unconstrained coupling efficiency reached the theoretical upper limit for a single etch design for the given SOI substrate layer cross section (while not resorting to more advanced subwavelength techniques), and the constrained design contributed a loss penalty of 0.08dB. The optimized grating coupler geometry was validated using 3D FDTD Lumerical simulations, and the coupling efficiency was comparable to within 0.5dB. In the future, 3D adjoint optimization seeded with the GC geometry, optimized with the 2D adjoint method, could be used to further improve the GC design.

Figure 6 shows a test device fabricated with the optimized single polarization GC, mentioned earlier, and a single microring resonator in an add-drop-thru configuration. The test device was probed with a SMF28 angled fiber array. From the thru transmission measurement, we estimated the GC to fiber coupling loss and 1dB bandwidth to be ~1.4dB and ~22nm, respectively. From the zoomed in view (1302-1320nm) of a single resonance wavelength, the thru response achieved an extinction ratio of ~10dB with a cavity Q of ~21,000, while the drop port had a loss of ~ 4dB, and the reflection measured from the add port was sufficiently low.



(a) (b) (c)

Figure 6: Fabricated silicon microring test device (a) optical microscope image, (b) thru, drop and add transmission spectra and (c) single resonance thru, drop and add transmission spectra.

3.2 Lens Chip

The microlenses were fabricated on 150mm diameter glass substrates CTE matched to silicon and designed to withstand multiple lead free solder reflow temperature cycles. The microlens arrays were recessed below the surface of the chip (Figure 7) to protect them during handling and to ensure the chip can be picked up with conventional flip chip tooling. Although each chip had 10 lenses, only the inner 8 were used. Their ROC variation across the wafer was <4%, while the intra-chip ROC variation was <0.3%, and the root mean squared (rms) surface roughness was <45nm. These values can be further improved as the fabrication process matures, and are within the value determined from our sensitivity analysis.

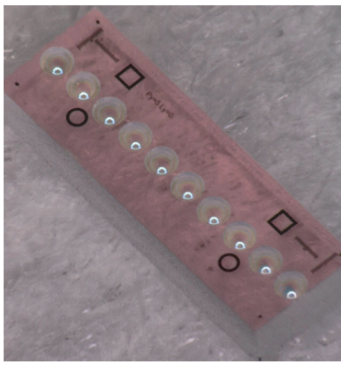
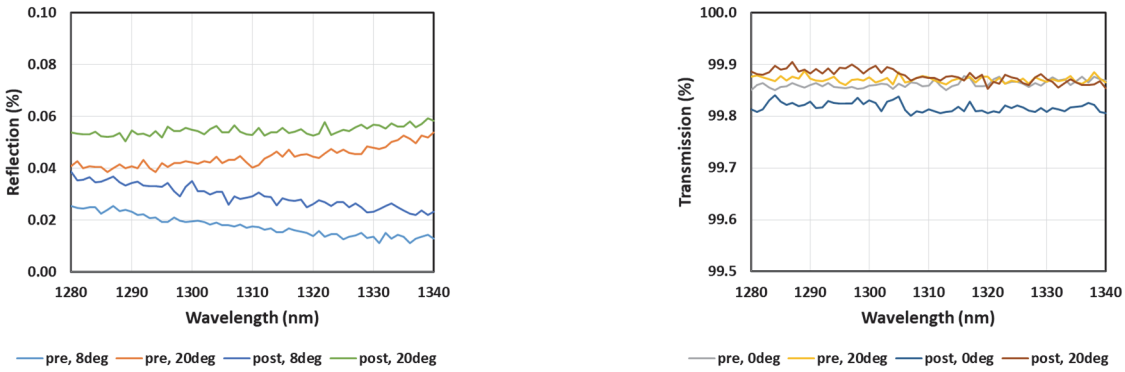


Figure 7: Optical microscope image of a fabricated 1x8 glass microlens array chip.

The lensed side of the wafer has a broadband antireflection coating (ARC). To verify the ARC can withstand multiple solder reflows, a test wafer with ARC on the front and back sides was subjected to three 270°C solder reflow cycles and inspected for delamination, cosmetic defects (such as cracks, bubbles, etc), and changes in reflection and transmission. Good adhesion and no cosmetic defects were observed pre or post thermal cycling. The reflection and transmission spectra were measured with a non-polarized broadband light source at two angles of incidence. The results are shown in Figure 8. There was a slight degradation in reflectance after 3X temperature cycles, but negligible change in transmission. Both reflection and transmission remained within their specification, <0.1% and >99.5%, respectively.

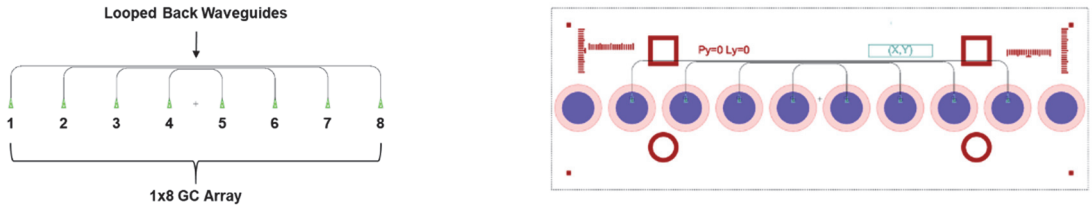


(a) (b)

Figure 8: Test wafer with ARC on the front and back sides. (a) Reflection and (b) transmission spectra measured at two angles of incidence, pre and post 3X 270°C solder reflow temperature cycling.

4. OPTICAL INTERFACE DEMONSTRATION

To demonstrate the optical interface, we took a two phase approach. In Phase 1, we fabricated a SiPh test structure with a 1x8 GC array and looped back waveguides from a standard CMOS foundry (Foundry A) process design kit (PDK). In Phase 2, we implemented the passive components for the DWDM microring SiPh transceiver, using our proprietary designs, at another CMOS foundry (Foundry B). The Phase 1 SiPh test structure from Foundry A is shown in Figure 9. GCs 1, 2, 3 and 4 are connected (or looped back) on-chip to GCs 8, 7, 6 and 5, respectively. The lens chip was affixed above the SiPh test structure, as shown in Figure 9. Notice that the lens array was offset with respect to the GC beam exit location to maintain the 8deg GC light beam exit angle after passing through the lens. Five test structures were assembled with lens chips, and the alignment accuracy of the GC and lens array was <5µm, perpendicular to the array direction.



(a) (b)

Figure 9: Schematic layout of the Phase 1, Foundry A, (a) SiPh test structure and (b) lens chip over the SiPh test structure.

A US Conec 1x8 expanded beam light turn ferrule was mounted in a fixture on the auto-aligner, discussed in section 2.4, and semi-actively aligned to each subassembly. The light path between the fiber ribbon terminated ferrule and SiPh was shown in Figure 5. Note that the optical socket and wedge adapter were not present in this experiment. Figure 10 shows the fiber to fiber insertion loss at 1310nm wavelength versus the looped back fiber channels (1-8, 2-7, 3-6 and 4-5). Based on these measurements and assuming the SOI waveguide loss is negligible, the fiber to SOI waveguide coupling loss (through the light turn ferrule, a microlens and GC) ranged from 2.3 to 4.5 dB.

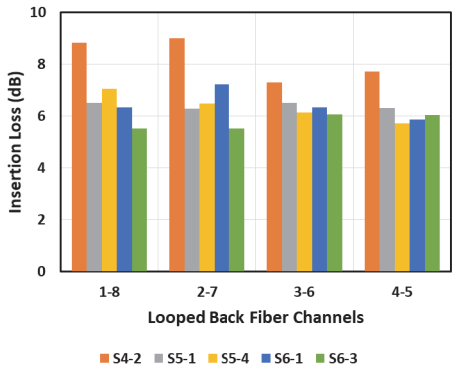


Figure 10: Fiber to fiber insertion loss vs looped back fiber channels for five Phase 1 (Foundry A) subassemblies semi-actively aligned to a 1x8 expanded beam light turn ferrule.

In Phase 2 at Foundry B, we implemented our proprietary passive silicon photonic building blocks (GC, microring, etc.) in a layout that resembles the DWDM SiPh transceiver. The fabricated chip is shown in Figure 11 and is designed with eight optical channels. A 1x8 GC array resides on the left side of the chip. The outermost channels (1 and 8, where 1 corresponds to the GC at the top of the array) are looped back with a relatively short SOI waveguide. A lens chip was affixed to the SiPh with ~2µm x-y alignment accuracy. Six different ferrules were semi-actively aligned to the subassembly using fiber channels 1 and 8 (corresponding to GCs 1 and 8). The wedge adapter and optical socket were not present in this experiment. As shown in Figure 12, the fiber to fiber insertion loss of the outermost fiber channels ranged from 4.7 to 6.3dB at 1310nm wavelength.

Figure 11: Optical image of the fabricated Phase 2 (Foundry B) test chip resembling the DWDM SiPh transceiver.

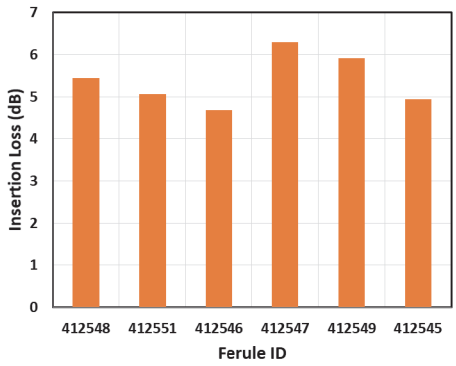
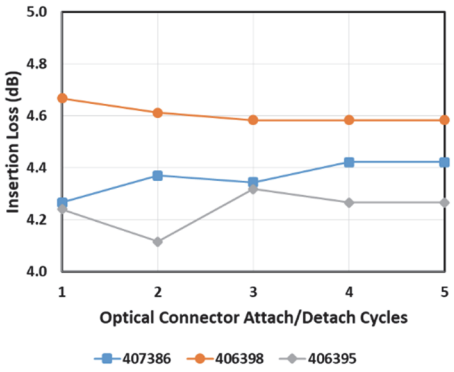


Figure 12: Fiber to fiber insertion loss between fiber channels 1 and 8 for six expanded beam light turn ferrules semi-actively aligned to the Phase 2 (Foundry B) subassembly.

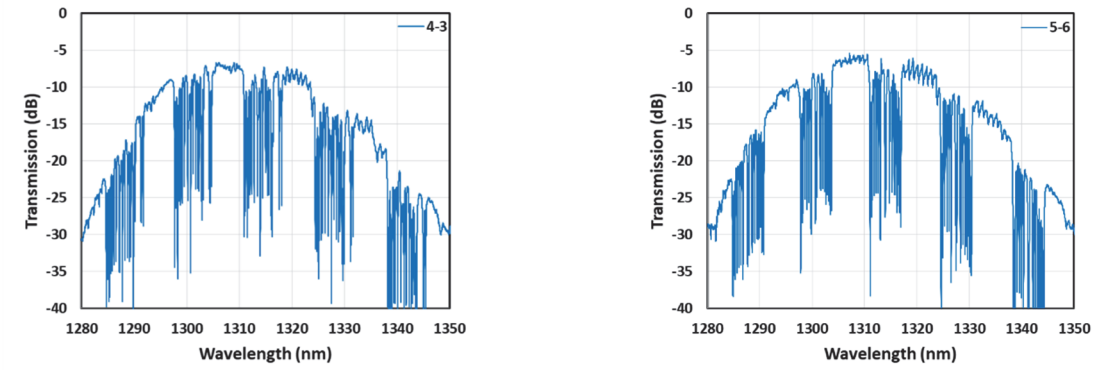
The Phase 2 subassembly was subsequently assembled with the optical socket and wedge adapter, as described in Section 2.4, to create the detachable optical interface. A photograph of the final assembly with the clip is shown in Figure 13. A critical requirement of detachable optical connectors is their ability to maintain consistent insertion loss after removal and reattachment. To demonstrate the insertion loss repeatability, three different ferrules were attached and detached five times each. The results are also shown in Figure 13. The maximum variation in fiber to fiber insertion loss of the outermost fiber channels (1 and 8) is 0.2dB. This particular assembly exhibited improved fiber to fiber insertion loss (< 4.7dB) compared to the experimental results in Figure 12.



(a) (b)

Figure 13: Detachable optical interface final implementation: (a) photograph and (b) fiber to fiber insertion loss repeatability test with three different expanded beam light turn ferrules.

Referring to Figure 11, channels 3 and 4, and 5 and 6 were linked by two long SOI waveguide buses, each coupled to 24 microring resonators. The fiber to fiber transmission spectrum of looped back fiber channels 4-3 and 5-6, with the optical connector attached, is shown in Figure 14. Note that the transmission curves represent the cascaded spectral response of all on-chip passive optical components, namely, two GCs, a long SOI waveguide and 24 microring resonators, as evidenced by the curvature of the overall envelope, added loss, and multiple resonant dips corresponding to each mirroring resonator along the waveguide bus.



(a) (b)

Figure 14: Fiber to fiber transmission spectrum of looped back fiber channels (a) 4 to 3 and (b) 5 to 6.

5. CONCLUSION

We presented our development efforts on a 1x8 SM detachable optical interface for DWDM microring SiPh transceivers. The optomechanical assembly includes a SiPh interposer, a solder reflow compatible surface mount glass microlens array chip, a machined wedge adapter, an injection molded solder reflow compatible optical socket, and an injection molded expanded beam SM light turn ferrule. The optical interface is separable in the expanded beam space where the x-y-z alignment is relaxed at the expense of angular alignment. Expanded beams mitigate losses associated with dust in the optical path and reduce the required optical connector to socket engagement and retention force compared to physical contact optical connectors. The optical interface was demonstrated on SiPh test chips manufactured at two different CMOS foundries with comparable insertion loss (<4.7dB at 1310nm wavelength). The complete detachable optical interface was implemented on a test chip, with our proprietary silicon photonic building blocks, whose layout resembles the DWDM microring SiPh transceiver. The fiber to fiber insertion loss ranged from 4.1 to 6.3 dB. A key requirement for detachable optical connectors is their ability to maintain consistent fiber to fiber insertion loss after multiple removals and reattachments. We successfully demonstrated 0.2dB insertion loss repeatability on the outermost channels (1-8) utilizing 3 different optical ferrules mated 5 times to the optical socket-wedge adapter mounted on the SiPh. With the ferrule

removed, SiPh transceivers enabled with our optical interface have the potential to be solder reflowed onto system boards with conventional surface mount equipment found in high volume outsourced semiconductor assembly and test facilities.

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